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REMARKS

In response to the Final Office Action mailed September 13, 2002, reconsideration is respectfully requested in view of the following remarks. To further the prosecution of this application, Applicants have addressed each of the issues raised in the Office Action, as discussed below.

In a telephone conference with the Examiner on January 13, 2003, the undersigned attorney of record explained to the Examiner that he must have misunderstood either the claim language or the principal reference, Da Franca. A discussion ensued, clearing up the Examiner's misunderstanding and resulting in agreement that, per Applicant's prior responses, Da Franca does not disclose charge sharing. Consequently, the rejection under 35 U.S.C. §102 will be withdrawn. The Examiner then indicated he would accept amendments to resolve the outstanding issues under 35 U.S.C. §112, in a response under 37 C.F.R. §1.116.

Claims 1-65 are now pending in this application, of which claims 1, 9, 12, 17, 21, 24, 27, 31, 34, 37, 38, 39, 58, 62, 63, and 64 are independent claims. In this response, claims 19, 20, 23, 26, 33, and 36 have been amended. The application as now presented is believed to be in allowable condition.

A. Objections to the Drawings

On page 2, the Office Action objects to the drawings, stating that the reference voltage Vref, discussed on line 30 of page 13 in connection with Fig. 5, is not shown. Applicants respectfully point out that the discussion of Fig. 5 on pages 12-13, and in particular on line 30 of page 13, merely discloses one particular possible group of connections according to one embodiment of the invention, stating that voltages V1, V3, V5, and V7, which are clearly shown in Figure 5, could be connected to a voltage Vref. It is well known in the art that any number of reference voltages could be used for connection to the voltage terminals shown in Fig. 5. Fig. 5 reflects this well known generality and as such is correct. It would not be appropriate to show Vref on Fig. 5. Therefore, Applicants respectfully request that this objection be withdrawn.

B. Amendments to the Specification

Several typographical errors were found in the specification, and have been corrected herein. First, the paragraph beginning at line 28 of page 9 was rewritten to correct a mistyped reference to mixer 72, which should have been mixer 74. Second, the paragraph beginning at line 21 of page 20 was rewritten to correct the mistyped reference numerals 148, 149, and 150, which should have been S48, S49, and S50. Finally, the paragraph beginning at line 31 of page 13 was rewritten to correct a mistaken reference to Figure 3 which should have been a reference to Figure 6. The specification is now believed to be correct.

C. Amendments to Drawings

Figures 4 and 5 have been amended to delete the spurious number label 152. Fig. 6 has been amended to include the waveform for P1 + P2, the logical OR of control signals P1 and P2. Figs. 17, 21-22, and 25 have been amended to delete the unnecessary element label "NC". Figs. 28A-B have been amended to correct an erroneous label; specifically, the label "P3" has been deleted and replaced with the label "P2". These amendments are clearly supported by the specification, as discussed below, and introduce no new matter.

D. Rejections Under 35 U.S.C. §112, First Paragraph

Claims 1-65 were rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicants respectfully traverse these rejections.

The Office Action states at paragraph 3a that "it is not understood what number 152 and elements QDAC1 to QDACN in Fig. 4 really are and how they are interconnected with the [sic] and the charge sharing network since they are not described in the specification." Fig. 4, which merely serves as an illustrative block diagram, is described on page 11, line 24 to page 12, line 2. As discussed in the specification, the block diagram of Fig. 4 demonstrates the manner in which the multi-bit digital input is related to the analog output. Namely, the analog outputs QDAC1 through QDACN of the block diagram show signals which are indicative of a sum of values in the multi-bit signal. The purpose of this figure was merely to demonstrate generically some possible relationships between the digital inputs and the analog outputs, which are discussed later

in more detail, along with the charge-sharing network. Therefore, it is believed that the specification does, in fact, describe all labeled elements of Fig. 4.

In paragraph 3b, the Office Actions states that "it is not understood what the number 152 in Fig. 5 really is since it is not described in the specification; it is not understood how switch S13 in Fig. 5 is controlled by P1 + P2 since the specification discloses that the P1 signal controls all switches S13-S16 (last line of page 13 and first line of page 14)." The Examine apparently misreads the quoted passage. It does not say that switch S13 is controlled only by the P1 signal, but instead says that the P1 signal controls switch S13. This is correct. It is also true that the P2 signal (which is "OR'd" with the P1 signal) controls switch s13. The Office Action has failed to mention that switch S13 is also described as being controlled by phase 2 of the three-phase clock on lines 10-12 of page 14, where it is stated that the switch S13 is closed during the P2 phase of the clock, along with switch S17, in order to provide an output to the output terminal 160. Thus, it is clear that one of the switches S13-S16, in this case S13, must be controlled by P1+P2 (i.e., the logical OR of P1 and P2), as is stated in the specification, in order to provide an output. Therefore, it is respectfully asserted that the operation and control of switch S13 is fully described in the specification and is consistent with the control signal shown in Fig. 5. While it is believed that Applicants have demonstrated ample support for the manner in which switch S13 is controlled, Fig. 5 has nonetheless been amended, as described above in the discussion of the amendments to the drawings, to explicitly show an additional signal which is derived from signals P1 and P2 and is the logical OR of those two signals.

In paragraph 3c, the Office Action states that "all equations on the right side of Figs. 7A-C, 8A-D and 12A-C, 14A-C, 19A-C, 33A-C and 24A-C are not understood since Vref is not shown in the drawings of the invention and Q(C1), Q(C2), Q(C3) and Q(C4) are not described in the specification." First, Applicants respectfully point out that it may be assumed that one skilled in any electrical art is familiar with the fact that the charge induced on a capacitor is equal to the capacitance of the capacitor times the voltage across the capacitor. This cannot be disputed. Consequently, using perfectly conventional notation, those skilled in the art will know that Q(C1) represents the charge (Q) on a capacitor C1, etc. Nonetheless, the specification has been amended in the paragraph beginning at page 14, line 13 to state that "the charges Q(C1)... Q(CN) represent the charge on capacitors C1... CN respectively." Secondly, Applicants point out that in the specification, reference is made to the fact the V1, V2, etc., which are stated in the

specification to be the inputs to the switched capacitor DACs such as those shown in Figs. 5, 13, 16, 27, etc., may each be connected to unique input voltages, or may all be connected to a common voltage level which is called Vref. An example of this explanation can be found at page13, lines 16-26. As is known to those of ordinary skill in the art, a standard logic level, such as Vref, may be used to represent a logical 1 or 0 in a digital computing environment. In that way, the same voltage Vref may be present on two bit lines even though one bit line represents a value an order of magnitude higher than the other. For instance, a higher-valued bit line may be coupled to a capacitor with a capacitance which is scaled in relation to the value that the bit line represents. There is no need to show a voltage labeled Vref in the drawing as the specification makes it clear the Vref is not a reference element and thus it does not come under 37 C.F.R. 1.84. Consequently, the facts discussed above, which are certainly known to those skilled in the art, coupled with the teachings of Applicant's specification, more than constitute support for the rejected.

The Office Action further states in its rejection that the switching ON/OFF operation of all the switches in each of Figs. 11-A-D, 12A-C, 14A-C, 15, 16A-E, 17-18, 19A-C, 20-22, 25, 27, 30, 33A-C and 34A-C is not understood since no switching control signal associated with each of the switches is shown in the drawings and is described in the specification. Applicants strongly disagree. For each figure, the discussion of that figure in the specification gives detailed information about the timing and control of the various switches in the figure with respect to the phase signals P1-P4, when applicable. In some cases, for instance in Fig. 15, switches whose timing and control information is not discussed are explicitly stated to serve purposes other than switching. In the case of Fig. 15, these switches serve to balance parasitic effects which could harm performance. In other cases, the switch timing and control of some figures is not discussed because the timing of the same switches has already been explained in connection with other figures, as is the case with Figure 16. Respectively, for Figs. 11, 12,14, 16-22, 25, 27, and 30, such discussions may be found at page 18, lines 1-24; from page 18, line 31 to page 19, line 13; page 20, lines 2-16; from page 23, line 5, to page 24, line 8; page 24, lines 13-34; from page 27, line 14 to page 28, line 16; and from page 32, line 5 to page 31, line 14. Thus, Applicants respectfully assert that the switching operations of each of the figures in the specification are fully supported and that no additional drawing figure or text is needed. If the Examiner contends

otherwise, he is respectfully requested to identify the specific switches whose controls, he believes, has not been adequately disclosed.

In paragraph 3e, the Office Action states that "it is not understood what element NC in Figs. 17, 21-22, 25 really is since it is not described in the specification." In response, the "NC" label has been removed, the control of the switches having been explained.

The Office Action states in paragraph 3f of the Office Action that "it is not understood what the four arrows on the right side of the scrambler 400 in Fig. 24 really are since they are not described in the specification." While Applicants respectfully assert that scramblers are well known to those skilled in the art of digital to analog conversion, and that figure 24 in conjunction with page 25, lines 21-32 is easily understood by any such person, the description of Fig. 24 beginning at page 25, line 21, has been amended to explicitly state that the scrambler "receives a three-bit digital input signal, bit_A, bit_B, bit_C, represented by the labeled arrows on the left, and outputs scrambled bits, represented by the arrows on the right."

The Office Action states that "it is not understood what the P3 in Figs. 28A-B really is since the specification discloses in line 5, page 30 that the conductor 454 is provided to supply the phase signal P2." Applicants have amended Figs. 28A-B to correct this typographical error. The description in the specification was correct as written, and Figs. 28A-B are now believed to agree with the specification.

In paragraph 3h, the Office Action states that "it is not understood what elements SCF, selectable gain, External CAP and Voltage output in Fig. 30 of the present invention really are since they are not described in the specification." The elements of Fig. 30 are described in the specification from page 31, line 6 to page 31, line 15. Fig. 30 is merely meant to provide an illustrative embodiment of the CT filter 92 shown in Fig. 2, and as such, is not described in great detail. However, Fig. 30 is fully described by the specification to the extent necessary to provide an exemplary embodiment of an element of the invention to those skilled in the art.

Finally, the Office Action states in paragraph 3i that "it is not understood what elements $P1 + bit_1 \cdot P2$, $P1 + bit_2 \cdot P2$, $P1 + bit_3$ P2 and $P1 + bit_4 \cdot P2$ in Fig. 31 really [are] since they are not described in the specification." Applicants disagree, and respectfully point out that Figures 33A-33C and 34A-34C, along with the relevant portions of the specification (page 32, line 5 to page 33, line 16) explicitly show the relationship between the control signals input to the various

switches of the squaring circuit in Figure 31 and the various clock phases P1-P3 and input bits bit_1-bit_4.

E. Rejections Under 35 U.S.C. §112, Second Paragraph

Claims 10, 19-20, 23, 26, 33, and 36 are rejected under 35 U.S.C. 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant respectfully amend in part and traverse in part.

In rejecting claim 10, the Office Action states that "it is not clear how more [sic] analog signals comprise exactly one signal." Claim 10 is directed toward the DAC of claim 9, wherein the one or more analog signals comprises exactly one signal. To put it simply, claim 9 is directed to at least one analog signal (one or more analog signals), while claim 10 further limits the claimed structure to exactly one output. There is no clearer way to state this and Applicants respectfully assert that claim 10 is allowable.

In rejecting claim 19, the Office Action asserts that there is no antecedent basis for the terms "the same value." Claim 19 is directed toward the method of claim 17, wherein the method further comprises connecting all of the capacitors together so each has substantially the same value. As discussed on page 8 of the Amendment mailed August 15, 2002, Applicants believe that there is clear antecedent basis for the limitations recited in claim 19. **However, the Examiner has failed to provide any indication that these arguments have even been considered**. Thus, although Applicants believe that the claim is allowable, they have amended it herein in an effort to render the claims clearer and expedite prosecution, and believe that it is now in condition for allowance.

The Office Action rejected claims 20, 23, 26, 33, and 36 under the assertion that there is no antecedent basis for the phrase "the same charge." Applicants respectfully disagree. As discussed on page 9 of the Amendment mailed August 15, 2002, Applicants believe there is clear antecedent basis for the term "the same charge." **Again, the Office Action has failed to provide any indication that these arguments have even been considered**. Once more, Applicants have nonetheless amended the claims in an effort to render them clearer and to expedite prosecution of the application. Each of claims 20, 23, 26, 33, and 36 is now believed to be in condition for allowance.

F. Rejections Under 35 U.S.C. §102

Paragraph 6 of the Office Action rejects claims 1-65 under 35 U.S.C. 102(b) as unpatentable over Da Franca et al., 5,008,674. Applicants respectfully traverse these rejections. As noted above, the Examiner has agreed, in the telephone interview, that the claims are not anticipated by Da Franca, and has stated he is withdrawing this rejection.

1. Office Action Fails to Note Previously Submitted Arguments

Applicants have previously submitted arguments addressing the rejection of each and every claim over Da Franca. These arguments are believed to distinguish each of the rejected claims over Da Franca and clearly place them in condition for allowance. The Office Action had failed to provide any indication that the previously submitted arguments were given consideration, which prompted the telephone interview. The Office Action failed to dispute any of the statements made in the previous Amendment. For example, the Office Action failed to dispute the fact that, contrary to statements in the Office Action that Da Franca discloses a state in which the capacitors CP0, CP1, and CPw-1 share charge with one another, there is no state or configuration of the devices shown in Da Franca in which the charge on any of CP0, CP1, and CPw-1 can influence the charge on or share charge with any of the other capacitors. Simply repeating the statement does not make it so.

If for any reason the Examiner does not withdraw the rejection Applicants respectfully request that the Examiner respond on the record to the previously submitted arguments. If they are believed to be deficient, Applicants request that the Office Action particularly point out any deficiency in the arguments. Otherwise, Applicants request that the rejection over Da Franca be withdrawn and claims 1-65 be allowed.

G. Provisional Double Patenting Rejection

Paragraph 9 of the Office Action states that claims 1-65 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting over claims 1-9 and 30 of copending Application No. 09/575,560.

Applicants note that this rejection is provisional and therefore does not require a response at this time. However, Applicants expressly reserve the right to respond at a future time.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicants' attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby request any necessary extension of time. If there is a fee occasioned by this response, including an extension fee that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

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X2/13/03

Marked-Up Specification

Please replace the paragraph beginning on line 28 of page 9 with the rewritten paragraph shown below:

--FIG. 1 is a block diagram of one embodiment of a portion of a handset 50 for a mobile communication system. The handset 50 includes an input portion having a transducer 54 that receives an input signal 56, e.g., a voice or other acoustical signal, representing information to be communicated via the mobile communication system. The transducer 54 converts the input signal 56 into an electrical signal, typically an analog signal, which is supplied to an analog-to-digital converter (ADC) 58, for example a voice band ADC. The ADC 58 periodically samples the electrical signal and generates a sequence of multi-bit digital signals, which are supplied to a digital baseband processor 60. The baseband processor 60 performs further signal processing, including for example, compression. The output of the baseband processor 60 is supplied to burst store stage 62, which feeds a GMSK modulator 64. The GMSK modulator 64 produces multi-bit digital signals, which is supplied via signal lines, represented by a signal line 66, to a digital to analog conversion system 68. The digital to analog conversion system 68 converts the sequence of multi-bit digital signals into an analog signal, which is supplied via signal line 70 to an output portion 72. The output portion 72 includes a mixer [72] 74 that receives the analog signal on signal line 70 and feeds a transmitter 76, which in turn transmits the signal. DAC can be used in any digital to analog conversion.--

Please replace the paragraph beginning on line 21 of page 20 with the rewritten paragraph shown below:

--FIG. 15 is a block diagram of another embodiment of the SC DAC 150, which is similar to the SC DAC 150 illustrated in FIGS. 9, 10A-10C, except that the SC DAC 150 of FIG. 15 further comprises a switch [148] S48, a switch [149] S49, and a switch [150] S50. A first terminal of the switch S48 is connected to the second terminal of the charge sharing switch S43. A first terminal of the switch S49 is connected to the second terminal of the charge sharing switch S45. A first terminal of the switch S50 is connected to the second terminal of the charge sharing switch S46. Each of the switches S48, S49, and S50 may, but need not serve one or more of the functions noted hereinbelow. In one embodiment, one purpose of the switches S48,

S49, S50 is to provide parasitic capacitance similar to that of output switch S47, so as to help cancel the effect of the parasitic capacitance of switch S47.--

Please replace the paragraph beginning at line 16 of page 20 with the following rewritten paragraph:

--FIG. 15 is a block diagram of another embodiment of the SC DAC 150, which is similar to the SC DAC 150 illustrated in FIGS. 9, 10A-10C, except that the SC DAC 150 of FIG. 15 further comprises a switch [148] S48, a switch [149] S49, and a switch [150] S50. A first terminal of the switch S48 is connected to the second terminal of the charge sharing switch S43. A first terminal of the switch S49 is connected to the second terminal of the charge sharing switch S45. A first terminal of the switch S50 is connected to the second terminal of the charge sharing switch S46. Each of the switches S48, S49, and S50 may, but need not serve one or more of the functions noted hereinbelow. In one embodiment, one purpose of the switches S48, S49, S50 is to provide parasitic capacitance similar to that of output switch S47, so as to help cancel the effect of the parasitic capacitance of switch S47.--

Please replace the paragraph beginning at line 31 of page 13 with the following rewritten paragraph:

--The DAC 150 may receive a non-overlapping 3-phase clock, P1, P2, P3, shown in FIG. [3] 6. The closed/open condition of the switches S3, S6, S9, and S12 is controlled by the P3 signal of the 3-phase clock. The P1 signal of the 3-phase clock controls the open/closed condition of the charge sharing switches S13, S14, S15, and S16. The P2 signal of the 3-phase clock controls the open/closed condition of the switch S17.--

Please replace the paragraph beginning at line 13 of page 14 with the following rewritten paragraph:

--FIGS. 7A-7C are block diagrams showing the operation of the SC DAC 150 of FIG. 5 for each of the 3 clock phases in the event that input terminals 172, 178, 184, and 190 are supplied with digital bit signals bit_1, bit_2, bit_3, bit_4, having logic states of 1, 0, 0, 0, respectively.

Tables show the relationship between the clock phase, and the state (i.e., voltage and charge) of the capacitors in the one-bit DACs. In Fig. 7 and similarly labeled figures, the charges Q(C1)... Q(CN) represent the charge on capacitors C1... CN, respectively. Referring now to FIG. 7A, on phase P3 of the 3-phase clock, all of the charge sharing switches S13, S14, S15, and S16 and the output switch S17, are in the open condition. The capacitor C1 is charged to V_{ref} in response logic state 1 on terminal 172. Capacitors C2, C3 and C4 are all discharged to ground in response to the logic state 0 signals on terminals 178, 184, 190, respectively. Referring now to FIG. 7B, on phase P1 of the 3-phase clock, all of the charging switches S3, S6, S9 and S12 (FIG. 5) and the output switch S17 are in an open condition, and all of the charge sharing switches S13, S14, S15 and S16 are in a closed condition, whereby charge is redistributed and resulting in the total charge on all of the capacitors being divided among all of the capacitors. If the capacitors C1, C2, C3, C4 all have the same capacitance value C, then the charge is shared equally so that the voltage across each capacitor becomes $V_{ref}/4$. Referring now to FIG. 7C, on phase P2, charge sharing switches S14, S15, and S16 are in the open condition, output switch S17 is in the closed condition, and capacitor C1 (FIG. 5) of one-bit DAC 162 delivers its charge to the output terminal 160. On the next occurrence of phase P3 (not shown), the multi-bit digital signal bit_1, bit_2, bit_3, and bit_4 may be updated and provided to the DAC 150 via input terminals 172, 178, 184, 190.--

Please replace the paragraph beginning at line 21 of page 25 with the following rewritten paragraph:

--FIG. 24 is a block diagram of one embodiment of a four bit scrambler 400 that receives a three-bit digital input signal, bit_A, bit_B, bit_C, represented by the labeled arrows on the left, and outputs scrambled bits, represented by the arrows on the right. A scrambler is typically most effective when all of the scrambler inputs receive data . The extra input(s) of the scrambler may for example be "hardwired" to a logic state, i.e., a 1 or a 0. In this event that an input(s) of a scrambler is hardwired, it may be desirable to hardwire a corresponding number of DAC input(s), to a logic state opposite to that used for the extra input(s) of the scrambler.--

Marked-Up Claims

19. (Amended) The method of claim 17, wherein the method further comprises connecting all of the plurality of capacitors together so [each] the value of each of the plurality of capacitors [has] is substantially [the] a same value.

20. (Amended) The method of claim 19, wherein [each of] the charge on each of the plurality of capacitors [has] is substantially [the] a same charge.

23. (Amended) The method of claim 21, wherein the method further comprises charging each of the plurality of capacitors to a level indicative of a value of correspondence and connecting all of the plurality of capacitors together so each of the capacitors has a charge which is substantially a [has the] same charge.

26. (Amended) The method of claim 24, wherein the method further comprises charging each of the plurality of capacitors to a level indicative of a value of correspondence and connecting all of the plurality of capacitors together so each of the capacitors has a charge which is substantially a [has] same charge.

33. (Amended) The DAC of claim 31 further comprising means for charging each of the plurality of capacitors to a level indicative of a value of correspondence and connecting all of the plurality of capacitors together so a charge of each of the capacitors is substantially a [has] same charge.

36. (Amended) The DAC of claim 34 further comprising means for charging each of the plurality of capacitors to a level indicative of a value of correspondence and connecting all of the plurality of capacitors together so a charge of each of the capacitors is substantially a [has] same charge.